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INTELLECTUAL PROPERTY
402-391-4448

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April 30, 2004

Commissioner for Patents
Box: 1450
Alexandria, VA 22313-1450

RE: APPLICATION OF SAYOOD ET AL., TITLED "SYSTEM AND METHOD FOR JOINT SOURCE-CHANNEL ENCODING, WITH SYMBOL DECODING AND ERROR CORRECTION";
SERIAL NO. 09/816,398;
FILE DATE: 03/24/2001;
ART UNIT: 2133;
EXAMINER: DIPAKKUMAR GANDHI.

Dear Sir;

I am in receipt of an Action dated 02/05/04 regarding the Application.

Please note that New Dependent Claims numbered 19 - 21 are added herein. In view of Cancellation of Original Dependent Claim 18, this brings the total Number of Pending Claims to Twenty (20), hence it is believed that no New Fees are required.

The Examiner has Rejected Claims 1-11 and 18, but Allowed Claims 12-16 with indication that Claim 18 will be Allowed upon correction of a spelling error. Herein Claim 18 is corrected and Amended into Claim 17, thereby putting Claims 12 - 17 in order for Allowance. Claims 1, 2, 3, 5, 7, 9, 10 and 11 are also Amended to better distinguish over the the art cited by the Examiner.

Attached hereto is a Declaration by the Inventors which the Examiner is respectfully requested to study prior to proceeding.

CERTIFICATE OF MAILING

I HEREBY CERTIFY THAT THIS TRANSMITTAL IS BEING DEPOSITED WITH THE UNTIED STATES POSTAL SERVICE WITH SUFFICIENT POSTAGE FOR FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO THE COMMISSIONER FOR PATENTS, BOX: 1450, ALEXANDRIA VA. 22313-1450 ON THE DATE INDICATED BELOW.

J. D. Welch 5/4/04

JAMES D. WELCH DATE

IN THE CLAIMS

Please Cancel Claim 18, Add New Claims 19 - 21, Continue Allowance of Claim 12 - 16 and Allow Amended Claim 17. Also, please reconsider and Allow Amended Claims 1 - 11, as Amended.

1. (currently amended): A variable length symbol, joint source-channel encoding, symbol decoding and error correction system comprising:

encoder system;
modulation-transmission means; and
combination sequential, and encoded symbol, decoding systems;

said encoder system comprising input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input thereinto;

said encoder system being functionally interconnected to said modulation-transmission means such that entry of a symbol to said encoder system results in said encoder means outputting an encoded sequence of bits therefore into said modulation-transmission means;

said modulation-transmission means and combination sequential, and encoded symbol, decoding systems being functionally interconnected such that an encoded symbol sequence of bits entered to said modulation-transmission means enters said combination sequential, and encoded symbol, decoding systems;

said sequential decoding system comprising a plurality of

bistable elements;

said encoded symbol decoding system comprising means for initiating an error correction routine to the end that, upon the detecting of the presence of an unexpected encoded reserved symbol a selection from the group consisting of:

at least one bistable element in said sequential decoding means is changed; and

selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means;

is performed;

wherein said reserved symbol is not allowed as an input symbol to said symbol ~~encoding~~ encoder system input means, and wherein the detection of the presence of an encoded allowed symbol by said encoded symbol decoding system does not initiate said error correction routine.

2. (currently amended): A variable length symbol joint source-channel encoding, symbol decoding and error correction system comprising:

encoder means;
modulation-transmission means; and
combination sequential, and encoded symbol,
decoding means;

said encoder means comprising input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input thereinto;

said encoder means further having means for generating, and in a sequence expected by said encoded symbol decoding means, outputting an encoded sequence of bits for at least one reserved symbol before and/or after an encoded allowed input symbol, which reserved symbol is not allowed as an input symbol to said encoder means input means;

said encoder means being functionally interconnected to said modulation-transmission means such that entry of a symbol to said encoder means results in said encoder means outputting an encoded sequence of bits therefore into said modulation-transmission means;

said modulation-transmission means and combination sequential, and encoded symbol, decoding means being functionally interconnected such that an encoded symbol sequence of bits entered to said modulation-transmission means enters said encoded symbol decoding means;

said sequential decoding means comprising a plurality of bistable elements;

said encoded symbol decoding means comprising means for initiating an error correction routine to the end that, upon the detecting of the presence of an unexpected encoded reserved symbol, or the absence of an expected encoded sequence of bits for a reserved symbol, a selection from the group consisting of:

at least one bistable element in said sequential decoding

means is changed; and

selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means;

is performed;

and wherein the detection of the presence of an encoded allowed symbol, other than by its coincidental presence in the place of an absent expected reserved symbol, by said encoded symbol decoding means, does not initiate said error correction routine.

3. (currently amended): A joint source-channel encoding, symbol decoding and error correction system comprising:

encoder means;
modulation-transmission means; and
decoding means;

wherein said encoder means comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input thereinto;

wherein said decoding means comprises a functional combination of a sequential decoder means which comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits, and an encoded symbol decoder means;

said encoder means being functionally interconnected to said modulation-transmission means and said modulation-transmission

means being functionally interconnected to said decoding means;

such that in use said encoder means receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof, said sequence of bits being caused to arrive at said decoding means;

and said encoded symbol decoder means having error detection means such that in use said encoded symbol decoder means, upon detecting the presence of an unexpected encoded sequence of bits for reserved symbol, initiates an error correction routine to the end that a selection from the group consisting of:

at least one bistable element in said sequential decoding means is changed; and

selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means;

is performed;

wherein said reserved symbol is not allowed as an input symbol to said ~~symbol-encoding~~ encoder means input means, and wherein the detecting of the presence of an encoded allowed symbol by said decoding means does not initiate said error correction routine.

4. (original): A joint source-channel encoding, symbol decoding and error correction system as in Claim 3 in which said encoder means is an arithmetic encoder and said decoding means comprises, as the encoded symbol decoder means, an arithmetic decoder.

5. (currently amended): A joint source-channel encoding, symbol decoding and error correction system comprising:

encoder means;
modulation-transmission means; and
decoding means;

wherein said decoding means comprises a functional combination of a sequential decoder means which comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits, and an encoded symbol decoder means;

wherein said encoder means comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input thereinto, said encoder means further having means for generating and, in a sequence expected by said encoded symbol decoder means, outputting an encoded sequence of bits for at least one reserved symbol before and/or after an encoded allowed input symbol, which reserved symbol is not allowed as an input symbol to said encoder means input means;

said encoder means being functionally interconnected to said modulation-transmission means and said modulation-transmission means being functionally interconnected to said decoding means;

such that in use said encoder means receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof in optional combination with a sequence of bits which represent at least one encoded reserved symbol in a pattern expected by said decoder means, said sequence of bits being caused to arrive at said decoding means;

and said encoded symbol decoder means having error detection means such that in use said encoded symbol decoder means, upon detecting the absence of an expected encoded reserved symbol, or the presence of an unexpected encoded reserved symbol, initiates an error correction routine to the end that a selection from the group consisting of:

at least one bistable element in said sequential decoding means is changed; and

selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means;

is performed;

and wherein the detection of the presence of an encoded allowed symbol, other than by its coincidental presence in the place of an absent expected reserved symbol, by said decoding means, does not initiate said error correction routine.

6. (original): A joint source-channel encoding, symbol decoding and error correction system as in Claim 5 in which said encoder means is an arithmetic encoder and said decoding means comprises, as the encoded symbol decoder means, an arithmetic decoder.

7. (currently amended): A joint source-channel encoding, symbol decoding and error correction system comprising:

arithmetic encoder system;
modulation-transmission means; and
decoding system;

wherein said arithmetic encoder system comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input thereinto;

wherein said decoding system comprises a functional combination of a sequential decoder system which comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits, and an arithmetic decoder system;

said arithmetic encoder system being functionally interconnected to said modulation-transmission means and said modulation-transmission means being functionally interconnected to said decoding system;

such that in use said arithmetic encoder system receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof, said sequence of bits being caused to arrive at said decoding system;

and said arithmetic decoder system having error detection means such that in use said arithmetic decoder system, upon detecting the presence of an unexpected encoded reserved symbol, initiates an error correction routine to the end that a selection from the group consisting of:

at least one bistable element in said sequential decoding means is changed; and

selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder

means;

is performed;

wherein said reserved symbol is not allowed as an input symbol to said ~~symbol-encoding~~ arithmetic encoder system input means, and wherein the detecting of the presence of an encoded allowed symbol by said decoding system does not initiate said error correction routine.

8. (currently amended): A joint source-channel encoding, symbol decoding and error correction system comprising:

arithmetic encoder means;
modulation-transmission means; and
decoding means;

wherein said decoding means comprises a functional combination of a sequential decoder means which comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits, and an arithmetic decoder means;

wherein said arithmetic encoder means comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input thereinto, said arithmetic encoder means further having means for generating and, in a sequence expected by said arithmetic decoder means, outputting an encoded sequence of bits for at least one reserved symbol before and/or after an encoded allowed input symbol, which reserved symbol is not allowed as an input symbol to said arithmetic encoder means input means;

said arithmetic encoder means being functionally interconnected

to said modulation-transmission means and said modulation-transmission m ans b ing functionally interconnected to said decoding means;

such that in use said arithmetic encoder means receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof in optional combination with at least one encoded reserved symbol in a pattern expected by said arithmetic decoder means, said sequence of bits being caused to arrive at said decoding means;

and said arithmetic decoder means having error detection means such that in use said arithmetic decoder means, upon detecting the absence of an expected encoded reserved symbol, or the presence of an unexpected encoded reserved symbol, initiates an error correction routine to the end that a selection from the group consisting of:

at least one bistable element in said sequential decoding means is changed; and

selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means;

is performed;

~~wherein said reserved symbol is not allowed as an input symbol to said symbol~~ and wherein the detection of the presence of an encoded allowed symbol, other than by its coincidental presence in the place of an absent expected res rved symbol, by said decoding means, does not initiate said error correction routine.

9. (currently amended): A method of correcting errors in decoded symbols which are encoded by an encoder means in a joint source-channel coding system, comprising the steps of:

a. providing a joint source-channel encoding, symbol decoding and error correction system comprising:

encoder means;
modulation-transmission means; and
decoding means;

wherein said decoding means comprises a functional combination of a sequential decoder means which comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits, and an encoded symbol decoder means;

wherein said encoder means comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input thereinto, said encoder means further having means for generating and, in a sequence expected by said encoded symbol decoder means, outputting an encoded sequence of bits for at least one reserved symbol before and/or after an encoded allowed input symbol, which reserved symbol is not allowed as an input symbol to said encoder means input means;

said encoder means being functionally interconnected to said modulation-transmission means and said modulation-transmission means being functionally interconnected to said decoding means;

such that in use said encoder means receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof, in optional

combination with at least one encoded reserved symbol in a pattern expected by said decoder means, said sequence of bits being caused to arrive at said decoding means;

and said encoded symbol decoder means having error detection means such that in use said encoded symbol decoder means, upon detecting the absence of an expected encoded reserved symbol, or the presence of an unexpected encoded reserved symbol, initiates an error correction routine to the end that a selection from the group consisting of:

at least one bistable element in said sequential decoding means is changed; and

selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means;

is performed;

wherein the detection of the presence of an encoded allowed symbol, other than by its coincidental presence in the place of an absent expected reserved symbol, by said decoding means, does not initiate said error correction routine;

b. inputting a plurality of symbols to the input means of said encoder means;

c. causing said encoder means to encode at least some of said plurality of symbols and output bits corresponding thereto into said modulation-transmission means;

d. causing said modulation-transmission means to enter said at least some of said plurality of encoded symbols into said functional combination of said sequential decoder means and encoded symbol decoder means;

e. causing said encoded symbol decoder means to, if detecting a present unexpected or absent expected, encoded reserved symbol, perform a selection from the group consisting of:

change at least one bistable element in said sequential decoder means; and

select a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means.

10. (currently amended): A method of correcting errors in decoded symbols which are encoded by an arithmetic encoder in a joint source-channel coding system, comprising the steps of:

a. providing a joint source-channel encoding, symbol decoding and error correction system comprising:

arithmetic encoder means;
modulation-transmission means; and
decoding means;

wherein said arithmetic encoder means comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input thereinto;

wherein said decoding means comprises a functional combination of a sequential decoder means which comprises a sequence of bistable

elements, each of which can be set to represent encoded symbol bits, and an arithmetic decoder means;

said arithmetic encoder means being functionally interconnected to said modulation-transmission means and said modulation-transmission means being functionally interconnected to said decoding means;

such that in use said arithmetic encoder means receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof, said sequence of bits being caused to arrive at said decoding means;

and said arithmetic decoder means having error detection means such that in use said arithmetic decoder means, upon detecting the presence of an unexpected encoded reserved symbol, initiates an error correction routine to the end that a selection from the group consisting of:

at least one bistable element in said sequential decoding means is changed; and

selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means;

is performed;

wherein said reserved symbol is not allowed as an input symbol to said ~~symbol-encoding-system~~ arithmetic encoder means input means, and wherein the detecting of the presence of an allowed encoded symbol by said decoding means does not initiate said

error correction routine;

b. inputting a plurality of symbols to the input means of said arithmetic encoder means;

c. causing said arithmetic encoder means to encode at least some of said plurality of symbols and output bits corresponding thereto into said modulation-transmission means;

d. causing said modulation-transmission means to enter said at least some of said plurality of encoded symbols into said functional combination of said sequential decoder means and arithmetic decoder means;

e. causing said arithmetic decoder means to, if detecting a present unexpected encoded reserved symbol perform a selection from the group consisting of:

change at least one bistable element in said sequential decoder means; and

select a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means.

11. (currently amended): A method of correcting errors in decoded symbols which are encoded by an arithmetic encoder in a joint source-channel coding system, comprising the steps of:

a. providing a joint source-channel encoding, symbol decoding and error correction system comprising:

arithmetic encoder means;

modulation-transmission means; and
decoding means;

wherein said decoding means comprises a functional combination of a sequential decoder means which comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits, and an arithmetic decoder means;

wherein said arithmetic encoder means comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input thereinto, said arithmetic encoder means further having means for generating and, in a sequence expected by said arithmetic decoder means, outputting an encoded sequence of bits for at least one reserved symbol before and/or after an allowed input symbol, which reserved symbol is not allowed as an input symbol to said arithmetic encoder means input means;

said arithmetic encoder means being functionally interconnected to said modulation-transmission means and said modulation-transmission means being functionally interconnected to said decoding means;

such that in use said arithmetic encoder means receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof in optional combination with at least one encoded reserved symbol in a pattern expected by said arithmetic decoder means, said sequence of bits being caused to arrive at said decoding means;

and said arithmetic decoder means having error detection means such that in use said arithmetic decoder means, upon detecting the absence of an expected encoded reserved symbol, or the presence of an unexpected encoded reserved symbol, initiates an

error correction routine to the end that a selection from the group consisting of:

at least one bistable element in said sequential decoding means is changed; and

selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means;

is performed;

wherein said reserved symbol is not allowed as an input symbol to said ~~symbol-encoding-system~~ arithmetic encoder means input means and wherein the detection of the presence of an allowed symbol, other than by its coincidental presence in the place of an absent expected encoded reserved symbol, by said decoding means, does not initiate said error correction routine;

b. inputting a plurality of symbols to the input means of said arithmetic encoder means;

c. causing said arithmetic encoder means to encode at least some of said plurality of symbols and output bits corresponding thereto, optionally intermingled with arithmetic at least one encoder means generated reserved symbol, into said modulation-transmission means;

d. causing said modulation-transmission means to enter said at least some of said plurality of encoded symbols, optionally along with at least one encoded reserved symbol entered into said

modulation-transmission means, into said functional combination of said sequential decoder means and arithmetic decoder means;

e. causing said arithmetic decoder means to, if detecting a non-present expected or present unexpected encoded reserved symbol, perform a selection from the group consisting of:

change at least one bistable element in said sequential decoder means; and

select a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means.

12. (original): A method of correcting errors in decoded symbols which are encoded by an arithmetic encoder in a joint source-channel coding system, comprises the steps of:

a. providing a joint source-channel encoding, symbol decoding and error correction, system comprising:

arithmetic encoder means;
modulation-transmission means; and
decoding means;

wherein said decoding means comprises a functional combination of a sequential decoder means which comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits, and an arithmetic decoder means;

wherein said arithmetic encoder means comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for

allowed symbols input thereinto, said arithmetic encoder means further having means for generating and, in a sequence expected by said arithmetic decoder means, outputting an encoded sequence of bits for at least one reserved symbol before and/or after an encoded allowed input symbol, which reserved symbol is not allowed as an input symbol to said arithmetic encoder means input means;

said arithmetic encoder means being functionally interconnected to said modulation-transmission means and said modulation-transmission means being functionally interconnected to said decoding means;

such that in use said arithmetic encoder means receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof in optional combination with at least one encoded reserved symbol in a pattern expected by said arithmetic decoder means, said sequence of bits being caused to arrive at said decoding means;

and said arithmetic decoder means having error detection means such that in use said arithmetic decoder means, upon detecting the absence of an expected encoded reserved symbol, or the presence of an unexpected encoded reserved symbol, initiates an error correction routine to the end that at least one bistable element in said sequential decoder means is changed;

b. entering a sequence of symbols into said arithmetic encoder such that said sequence of symbols are encoded and exited therefrom as a binary bit stream sequence of $+\underline{x}\sqrt{E_s}$ and $-\underline{x}\sqrt{E_s}$ signals, corresponding to a string of "1"/("0")'s and "0"/("1")'s which pass through said transmission channel and enter said sequential decoder means, where $\underline{x}$ is a fraction;

c. making hard logic circuitry decisions as to the presence of "1"/("0")'s and "0"/("1")'s based on said binary bit stream sequence of $+\underline{x}\sqrt{E_s}$ and $-\underline{x}\sqrt{E_s}$ signals while identify decisions based upon signals wherein $\underline{x}$ is of a value so as to cause the values of $+\underline{x}\sqrt{E_s}$ or $-\underline{x}\sqrt{E_s}$ to be within a null zone of $+\Delta$ to $-\Delta$ around 0.0, and identifying said decisions as "branch point" decisions in said sequential decoder means ;

d. monitoring output from said arithmetic decoder for errors and when an error is indicated thereby, identifying a "branch point" in said sequential decoder means and correcting the "1"/("0") or "0"/("1") based binary bit thereat by inverting it to "0"/("1") or "1"/("0").

13. (original): A method of correcting errors in decoded symbols as in Claim 12, in which in step d. involves the determination of the presence or absence of non-alphabet symbols other than as expected, said non-alphabet symbols being not-allowed as arithmetic encoder input symbols.

14. (original): A method of correcting errors in decoded symbols as in Claim 12, which comprises practicing step d. more than once, with said error correcting method further comprising the step of:

e. defining a tolerable Hamming distance threshold Tc, and keeping count of the number Kc of "branch points" in said sequential decoder means at which correction of the "1"/("0") or "0"/("1") based binary bit thereat by inverting to "0"/("1") or "1"/("0") has been performed; and

if Kc exceeds Tc, expanding the null zone by increasing the magnitude of Δ , thereby making available additional "branch points".

15. (original): A method of correcting errors in decoded symbols as in Claim 14, said error correction method further comprising the step of:

f. determining in a second or greater practice of step e. if the identified "branch point" is sequentially prior to the "branch point" identified in the immediately previous practice of step e. and if so decreasing the value of Kc by 1, otherwise increasing the value of Kc by 1.

16. (original): A method of correcting errors in decoded symbols as in Claim 12, which comprises practicing step d. more than once, with said error correcting method further comprising the step of:

e. defining a means for calculating a Euclidean distance between received and decoded symbols, and a tolerable rate of increase of Euclidean distance between sequential practice of step d., and

if said Euclidean distance increases faster than at said tolerable rate, expanding the null zone by increasing the magnitude of Δ , thereby making available additional "branch points".

17. (currently amended). A method of correcting errors in decoded symbols which are encoded by an arithmetic encoder in a joint source-channel coding system, comprises the steps of:

a. providing a joint source-channel encoding, symbol decoding and error correction system comprising:

arithmetic encoder means;

modulation-transmission means; and
decoding means;

wherein said decoding means comprises a functional combination of a sequential decoder means which comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits, and an arithmetic decoder means;

specific bistable elements in said sequential decoder means being identified as fixed branch points;

wherein said arithmetic encoder means comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input thereinto, said arithmetic encoder means further having means for generating and, in a sequence expected by said arithmetic decoder means, outputting an encoded sequence of bits for at least one reserved symbol before and/or after an encoded allowed input symbol, which reserved symbol is not allowed as an input symbol to said arithmetic encoder means input means;

said arithmetic encoder means being functionally interconnected to said modulation-transmission means and said modulation-transmission means being functionally interconnected to said decoding means;

such that in use said arithmetic encoder means receives a sequence of allowed symbols at its input means and provides an encoded sequence of bits for at least some thereof in optional combination with at least one encoded reserved symbol in a pattern expected by said arithmetic decoder means, said sequence of bits being caused to arrive at said decoding means;

and said arithmetic decoder means having error detection means such that in use said arithmetic decoder means, upon detecting the absence of an expected encoded reserved symbol, or the presence of an unexpected encoded reserved symbol, initiates an error correction routine to the end that:

> selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means at said specified branch points;

is performed;

b. entering a sequence of symbols into said arithmetic encoder means such that said sequence of symbols are encoded and exited therefrom as a binary bit stream sequence;

c. monitoring output from said arithmetic decoder means for errors;

d. upon detection of an error by said arithmetic decoder means, producing a plurality of series of sequential bits which result from the changing of bistable elements in said sequential decoder means at said branch points by using fixed branch point bistable elements in said sequential decoder means;

e. determining which series of sequential bits in said produced plurality of series of sequential bits is most likely correct <u>utilizing at least one selection from the group consisting of:</u>

<u>1. eliminating any series of sequential bits which contains an encoded reserved symbol;</u>

2. applying a metric to at least two series of sequential bits which do not contain an encoded reserved symbol, to determine which of said at least two series of sequential bits is most likely correct;

3. applying an Euclidean metric to at least two series of sequential bits which do not contain an encoded reserved sysbol, to determine which of said at least two series of sequential bits is most likely correct.

18. (canceled):

19. (new): A method as in Claim 9, wherein said encoded reserved symbol is selected from a group of at least two reserved symbols, and wherein at least two different expected reserve symbols are selected and entered into said modulation-transmission means.

20. (new): A method as in Claim 10, wherein said encoded reserved symbol is selected from a group of at least two reserved symbols.

21. (new): A method as in Claim 11, wherein said encoded reserved symbol is selected from a group of at least two reserved symbols, and wherein at least two different expected reserve symbols are selected and entered into said modulation-transmission means.

DISCUSSION

Because it is very important, it is first presented that all known art teaches initiation of error correction by an encoded symbol decoding system upon detection of an ---allowed symbol---. Only the present Specification teaches detection of the presence of unexpected or absence of expected---reserve symbols---to initiate error correction. It is acknowledged that when an expected reserve symbol is absent that an allowed symbol can appear as present in its place, but that is different from an allowed symbol initiating error. In such a case, regardless of the appearance, it is the absence of an expected reserve symbol that initiates error detection. The allowed symbol itself does not initiate error detection. Most Independent Claims are Amended herein with language such as:

> and wherein the detection of the presence of an allowed symbol, other than by its coincidental presence in the place of an absent expected reserved symbol, by said encoded symbol decoding system, does not initiate said error correction routine;

to add this required limiting interpretation.

In addition, New Claims 19 - 21 are added which further describe "reserved symbols", and, although considered unnecessary, Applicant would consider importing them into the Independent Claims from which they Depend if the Examiner can provide explanations to why such should be required.

Continuing, regarding the Rejected Claims, as the Examiner is aware, in view of the teaching in Graham v. John Deere Co. an Applicant's Application can not be used as a teaching reference.

Many Cases could, of course be cited, but a quote from ATD Corp. v. Lydall, Inc. 159 F.3rd 534, 48 USPQ2d 1321 (Fed Cir. 1998) suffices to make the point, said quote being:

> "Determination of obviousness can not be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the invention".

To expand, Patent Application Examination can not be conducted in hindsight using the Applicant's Specification and Claims as the teachings to guide the seeking out of elements missing in a primary reference. There must be teachings in "a" prior art reference which teach what elements to seek out and how to modify and combine said elements found in other references, to arrive at the Claimed invention. The simple existence of elements in other references which arguably could be modified and combined to arrive at a new invention is not sufficient to make a new invention obvious in the absence of instructive guiding insight in "a" reference. In that light, it is stated that the Sayood et al. Article does not even remotely suggest that elements found in the various identified Patents should be sought out, modified and combined with elements disclosed in the Sayood et al. Article. Further, the references identified by the Examiner disclose many elements in addition to those identified by the Examiner, and nothing in Sayood et al. or in any cited reference provides the instructions as how to reject said additional elements when selecting other elements. Again, the teachings of an Applicant's Application can not be used as a guide to what elements are missing in a primary reference, and then seek said elements in other references and then, without teachings other than in the Applicant's Application, hold that would be obvious to arrive at the Applicant's invention because said elements have been identified. Such a procedure is evidence of the use of prohibited hindsight.

It is noted at this point that the Declaration of the Inventors presented herein makes clear that adding elements found in modified form in the various references (eg. Doshi et al. and Eerenstein et al.), which elements are missing in, and not even suggested in the Sayood et al. Article cited by the Examiner, would render the Sayood et al. teachings inoperable. The Sayood et al. Article teaches a very different invention, one which can not be easily modified to provide the presently Claimed invention.

As New Claims are entered herein, support thereof is identified on Page 20, beginning in Line 11 where it states:

> It is another purpose of the present invention to disclose use of reserved symbols as means to enable encoded symbol, decoding means, (arithmetic decoder), to identify errors, said identified errors being corrected by the changing of at least one bit is an associated sequential decoder means.

Note the wording "reserved symbols", which indicates the use of more than one symbol.

REGARDING SPECIFIC CLAIMS

CLAIM 1.

Regarding Claim 1, the Examiner has provided no indication as to how Sayood et al., or other cited reference, provides direction, or even suggestion, which would lead one skilled in the art to seek out to seek out Doshi et al. and Eerenstein et al., and then, while rejecting most elements therein, identify therein the presence of elements which provide means to overcome admitted

deficienci s in Sayood et al:

the specific use of the modulation-transmission means and combination sequential, and encoded symbol, decoding system being functionally interconnected such that an encoded symbol sequence of bits entered to the modulation-transmission means enters the combination sequential, and encoded symbol, decoding system;

the specific use of a sequential decoding system;

the presence of an unexpected encoded reserve symbol, wherein the reserve symbol is not allowed as an input symbol to the symbol encoding system;

a system comprising a plurality of bistable elements and a selection from the group consisting of:

at least one bistable element in said sequential decoding means is changed; and

selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means;.

Only the Applicant's Application provides teachings which would have guided the Examiner to identify Doshi et al. and Eerenstein et al., and as mentioned, use thereof as a teaching reference is prohibited in the Examination procedure.

CLAIM 2

A specific point which must be addressed as it seems to be a point of confusion, is that the "Framing Byte" in Doshi et al., is absolutely not an "Encoded Reserve Symbol" as that terminology is used in the present teachings. The Doshi et al. "Framing Byte" is an --allowed symbol-- in the Doshi et al. teachings, emphasis added. Said Doshi et al. Framing Byte is expected in the Doshi et al. teachings and it is also noted that it always consists of the same bits. (Note, Claim 2, along with others herein, are Amended in this Response to stress and make definite in said Claims what is believed establishes itself, without more, a Patentable distinction over the prior art, said Amendment being appropriately selected from:

> , and wherein the detecting of the presence of an allowed symbol by said encoded symbol decoding system does not initiate said error correction routine; and

> , and wherein the detection of the presence of an allowed symbol, other than by its presence in the place of an expected reserved symbol, by said encoded symbol decoding system does not initiate said error correction routine.

Further, Claims 19 - 27 are added in this Response, and Applicant will consider entering them into their Parent Claims if necessary to secure Allowance. Said Claims make clear that present invention "reserved symbols" do not always consist of the same bits.

The Examiner states that Doshi et al. also teaches a sequential decoding means and means for initiating an error correcting routine to the end that, upon the detecting of the presence of an unexpected encoded reserved symbol, or the absence of an encoded sequence of bits for a reserved symbol (FEC decoder 255 in figure 2, Col. 2 lines 64-67, Doshi et al.), and that

Eerenstein et al. teach a system comprising a plurality of bistable elements; and a selection from the group consisting of:

> at least one bistable element in said sequential decoding means is changed; and
>
> selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means;

is performed (figure 1, col 3, lines 46-48, col. 4, lines 1-3, col. 7, lines 30-59, col. 8, lines 1-2 Eerenstein et al.).

However, the Examiner does not identify any teachings other than in the present Application, (use of which is prohibited), which would have guided one skilled in the art to, without undue experimentation and invention, identify Doshi et al. and Eerenstein et al., and while rejecting other elements therein, select the elements the Examiner identifies, and then modify said selected elements and incorporate them into the teachings of Sayood et al. to arrive at the present invention. To arrive at a functioning present invention system given only Sayood et al., is an undertaking is not at all obvious, even if it is conceded that Doshi et al. and Eerenstein et al. might be known to one skilled in the art, because there are no teachings in any reference, except the present Application, as how to identify elements missing in Sayood et al. as present in Doshi et al. and Eerenstein et al., and then how to select them while rejecting other elements present in Doshi et al. and Eerenstein et al., and then modify the selected elements in Doshi et al. and Eerenstein et al. and functionally integrate them into the teachings of Sayood et al. to arrive at a functioning present invention.

Without the present Application as a guide, use of which, again, is prohibited as a teaching guide, there is a "magic wand" step involved in the Examiner's argument, which "magic" is certainly not within the scope of what would be obvious to one skilled in the art as that terminology is typically used.

CLAIM 3

The Examiner argues that Sayood et al teaches a joint source-channel encoding, symbol decoding and error correction system comprising encoder means, modulation-transmission means, and a decoding mens; wherein said encoder means comprises input means for accepting a sequential plurality of allowed input symbols and output means for outputting an encoded sequence of bits for allowed symbols input thereto.

The Examiner then argues that Doshi et al., teach the decoding means comprises a functional combination of a sequential decoder means and an encoded symbol decoder means as recited in Claim 3 of the present Application:

> wherein said decoding means comprises a functional combination of a sequential decoder means which comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits, and an encoded symbol decoder means;

To support this the Examiner cites Doshi et al. Col. 17, Lines 56-59 to support this view. However said Doshi et al. Col. 17, Lines 56-59 actually state:

> ...The exact number of decoders at the receiver may be one, as described herein with respect to sequential decoding or greater, if parallel decoding is desired. The quantity of

decoders employed at individual CMs ultimately is a design decision made by the engineer...

The Examiner also cites Doshi et al. Col 2, Lines 64-67 in further support of his position. Said Doshi et al. Col 2, Lines 64-67 state:

> At the receiver, data is first decoded and then descrambled. Therefore, FEC is utilized at the receiver to identify and correct bit errors introduced during transmission, prior to a received bit error being descrambled,

Applicant simply does not understand how one skilled in the art finds even a remote suggestion in Sayood et al. as how to seek out Doshi et al., then focus on the cited Doshi et al. Col. 17, Lines 56-59 and Col 2, Lines 64-67 and conclude that the identified Doshi et al. recitals obviate:

> a decoding means which comprises a functional combination of a sequential decoder means which comprises a sequence of bistable elements, each of which can be set to represent encoded symbol bits, and an encoded symbol decoder means;

Even assuming one skilled in the art did somehow find the Examiner cited Doshi et al. recitals, how would he or she know to select a sequential rather than parallel decoding approach based in the Doshi et al teachings, and why would he or she choose to completely ignore the Doshi et al. emphasis on decoding prior to descrambling. ONLY the Present Application provides the teachings that guided the Examiner is the formulation of his position, and as is the theme of the Response, that is simply a forbidd n approach to Examination.

As for Eerenstein et al. teaching additional limitations, Applicant does not understand how one skilled in the art would be led to said Eerenstein et al. Patent based on what is found in Sayood et al. even in view of Doshi et al. But assuming that somehow did occur, it is absolutely not understood how the cited language in Eerenstein et al. remotely leads one skilled in the art to provide, as Claim 3 of the present Application recites:

> an error correction routine to the end that a selection from the group consisting of:
>
> > at least one bistable element in said sequential decoding means is changed; and
> >
> > selection is made of a series of sequential bits, said selection being made from a group consisting of a plurality of such series of sequential bits which result from the changing of bistable elements in said sequential decoder means;
>
> is performed;

The language cited by the Examiner from Eerenstein et al. is:

Col. 1, Lines 48-68:

> The invention will be described in detail hereinafter with reference to the sequential finite-state machine with reference to the sequential finite-element machine whose state transition diagram is shown in Fig. 1. The FSM has 16 states and various transitions therebetween which are controlled by a clock signal and an input signal. The input signal is in this case a bivalent type ("0" or "1"). Generally speaking, an input signal may also consist of more

> bits. At instants which are defined by the clock signal, the finite-state machine changes over to a next state, The state bearing the number 1 is absorbing in the case of 5 successive input signals having the value "1": the rest state 1 is reached from any rest state after at the most 5 ones of the input signal{c(0), c)1),..., c(X-1)} in this case appears as follows:{"1", "1", "1", "1","1"}; X=5 and N=4. It will be apparent that those values have been chosen merely by way of example; other choices are also possible. This sequential finite-state machine can be implemented in a circuit by means of 4 bistable elements or flipflops (2 to the power of 4 implies 16 feasible states), and a set of combinatory logic which relates the correction transitions between the states.

The language in Eerenstein et al. at Col. 7, Lines 30-59 and Col. 8 Lines 1-2 is no more enlightening than that just recited as to how the Examiner was led to Eerenstein et al. based upon Sayood et al., and even if some reasonable pathway could be established as to how Eerenstein et al. was identified, Applicant does not understand how the cited language therein obviates the relevant portion of Claim 3 of the present Application.

CLAIM 5

The theme of the foregoing is incorporated here. Nothing in Sayood et al. would lead one skilled in the art to seek out Doshi et al. Additionally, the Examiner cited language from Doshi et al. in Col 1, Lines 42-43 states:

> Typically, FEC is implemented by applying an algorithm to data to generate redundant bits at the transmitter, performing the same algorithm on the data at the receiving end, and comparing the transmitted calculation with the received calculation.

Applicant does not understand how the language "generate redundant bits" obviates "accepting a sequential plurality of allowed input symbols". There is nothing which would lead one skilled in the art to consider that the language "generate redundant bits" from Doshi et al. obviates the procedure of "accepting a sequential plurality of allowed input symbols" from the present Application. And even is some connection could be shown there is still no relationship between the language "reserved symbol" and "redundant bits". In fact, a present Application "reserved symbol" is not redundant with allowed symbols. Further, accepted definition of the word "bits" is not necessarily identical with "symbols".

Additional similar argument could be presented but it is felt unnecessary at this point.

CLAIMS 4 AND 6

The Examiner states that Sayood et al. and Doshi et al. do not specifically teach the claimed invention described in Claims 3 and 5 are Arithmetic Encoder and decoder means and cites Kimura et al. to provide the missing limitation. Again, it is not understood how Sayood et al. leads one to find Kimura et al. except by using the present Application as a teaching reference.

CLAIMS 7 - 11

Applicants feel at this point that in view of the Declaration provided thereby, and in view of it being forbidden to use an Application as a teaching reference, in combination with demonstrated application thereof to Claims 1 - 6, it is not necessary to counter each Examiner point. In general the

Examiner's approach of simply identifying many references which variously contain some arguably relevant elements, but which references also each contain many other non-relevant elements, and then arguing that it would be obvious to select certain arguably relevant elements while rejecting the many non-relevant elements, and then modifying the selected elements and combining them in a way to arrive at the present invention, is not proper Examination Procedure. The Examiner has not provided a reference which guides said efforts via teachings which one skilled in the art could follow without undue experimentation. The Examiner's approach would provide avenue to find any invention obvious. Again, there must be teachings in "a" reference which would specifically lead one skilled in the art to seek out the elements missing in said teachings and include them in said teachings in a manner leading to an invention. There are an infinite number of inventions possible in view of the elements present in the reference cited by the Examiner, and nothing what-so-ever, present anywhere except in the Application, (which can not be used as a teaching reference), guides production of the specific invention Claimed in the present Application.

For emphasis---without teachings in a reference suggesting how to modify teachings therein to arrive at a new invention, it is not proper to determine obviousness to arrive at a new combination of elements based upon the simple existence of elements which are somehow similar being applied in different inventions. To hold otherwise would literally render substantially every new invention obvious because the elements thereof in modified form are variously to be found scattered in many references.

Applicant points out that Claims 9, 10 and 11 are method Claims which allow new use for existing systems. Even if the system were found obvious, (which Applicant argues herein has not

been established under Allowed Examination procedure), they can not be rejected based thereupon. There is absolutely no reference except the present Application which recites the sequence of steps Claimed. There is absolutely no reference that even comes close to reciting the sequence of steps.

Finally, again, the Applicant feels the Examiner has used the Applicant's Application as a Teaching Reference to provide the concept of "reserved symbols", which and on its own establishes Patentability. It is again noted that the language:

> , and wherein the detecting of the presence of an allowed symbol by said encoded symbol decoding system does not initiate said error correction routine; and
>
> , and wherein the detection of the presence of an allowed symbol, other than by its presence in the place of an expected reserved symbol, by said encoded symbol decoding system does not initiate said error correction routine.

is Amended into Claims 1, 2, 3, 5, 7, 8, 9, 10 and 11 as appropriate. Support therefore is found on Page 8, Lines 1 - 5 of the Specification as Originally Submitted. This is language is specifically stated to draw differentiation between what is meant by "reserve symbol" and "allowed symbol" in the present invention. The prior art does not teach use of "reserve symbols", especially where a reserved symbol is not allowed as an input symbol to said symbol encoding system. Errors in prior art are determined by various techniques applied to "allowed symbols" which have become modified by encoding and transmission.

Applicant accepts Allowance of Claims 12 - 17 (as Amended), request that Claim 18 be Canceled, and respectively requests that Claims 1 - 11 (as Amended), and New Claims 19 - 21 be considered and Allowed in view of Applicant's Declaration and in view of proper Examination Procedure which prohibits use of hindsight.

Should problems remain please contact me by phone if that would expedite the efforts. Applicants are open to Examiner suggestion and amendment.

Sincerely,

JAMES D. WELCH

JW/hs

enc. Declaration of Applicants